KPR Institute of Engineering and Technology

Learn Beyond

(Autonomous | Affiliated to Anna University)

POSTGRADUATE PROGRAMMES

CURRICULUM AND SYLLABI

PROGRAMME

M.E. | VLSI Design

REGULATIONS

2026

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I. Vision and Mission of the Institute

Vision

To become a premier institute of academic excellence by imparting technical, intellectual and professional skills to students for meeting the diverse needs of industry, society, the nation and the world at large

Mission

- Commitment to offer value-based education and enhancement of practical skills
- Continuous assessment of teaching and learning processes through scholarly activities
- Enriching research and innovation activities in collaboration with industry and institutes of repute
- Ensuring the academic processes to uphold culture, ethics and social responsibilities

II. Vision and Mission of the Department

Vision

To be a centre of excellence in education, research, and innovation in Electronics Engineering with specialization in VLSI Design and Technology to meet the evolving needs of society

Mission

The mission of the department is to

- Develop competencies in Electronics Engineering and VLSI Design through skill- based education in collaboration with industry
- Foster research, innovation, and entrepreneurship to develop sustainable solutions for societal needs
- Inculcate professionalism, ethical values, leadership, and lifelong learning

III. Program Educational Objectives (PEOs)

The Program Educational Objectives (PEOs) of the VLSI DESIGN (VL) represent major accomplishments that the graduates are expected to achieve after two years of graduation.

PEO1: Analyze and solve complex VLSI circuits and systems through the acquired in-depth knowledge

PEO2: Develop managerial skills and apply appropriate tools in the domains of VLSI design incorporating safety, sustainability and become a successful professional

PEO3: Exhibit professionalism while communicating with local, national and foreign peers bound with regulations and leading life- long learning

IV. Program Outcomes (POs)

Graduates of the VLSI DESIGN will be able to

PO1: An ability to independently carry out research/investigation and development work to solve practical problems

PO2: An ability to write and present a substantial technical report/document

PO3: An ability to demonstrate a degree of mastery over VLSI Design and Analysis

PO4: An ability to apply advanced concepts of VLSI for chip design with state of art tools

PO5: An ability to evolve customizable Chip Design for different Engineering applications

PO6: An ability to provide paradigm solution in the development of customized prototypes and chip design which have social and global relevance

V. PEO / PO Mapping

Following three levels of correlation should be used:

1: Low

2: Medium

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3: High

Particular	PO1	PO2	PO3	PO4	PO5	PO6
PEO 1	3	1	3	3	3	2
PEO 2	2	2	2	3	3	3
PEO 3	2	3	2	2	2	3

VI. Mapping of Course Outcomes (COs) with Program Outcomes (POs)

Sem	Course Title	PO1	PO2	PO3	PO4	PO5	PO6
I	Graph Theory and Optimization Techniques	✓	✓	✓	-	-	-
	System Verilog Techniques	✓	✓	✓	✓	✓	✓
	Semiconductor Device Modeling	✓	✓	✓	✓	✓	✓
	Digital System Design with AI for VLSI	✓	✓	✓	✓	✓	✓
	Research Methodology and IPR	✓	✓	-	-	-	✓
	HDL Programming Laboratory	✓	✓	✓	✓	✓	✓

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VLSI DESIGN

Regulation 2026

For the students admitted from 2026 onwards

CHOICE BASED CREDIT SYSTEM

CURRICULUM FOR I - IV SEMESTERS

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SEMESTER I

No	Course Code	Title	Category	Type	L	T	P	J	C
1	P26MA103	Graph Theory and Optimization Techniques	FC	TwL	2	-	2	-	3
2	P26VL101	System Verilog Techniques	PCC	T	3	-	-	-	3
3	P26VL102	Semiconductor Device Modeling	PCC	T	3	-	-	-	3
4	P26VL103	Digital System Design with AI for VLSI	PCC	T	3	-	-	-	3
5	P26RMC01	Research Methodology and IPR	RMC	T	3	-	-	-	3
6	P26VL104	HDL Programming Laboratory	PCC	L	-	-	4	-	2
7	-	Professional Elective - I	PEC	T	3	-	-	-	3
Total									20

T - Theory, **L** - Laboratory, **TwL** - Theory with Laboratory, **TwP** - Theory with Project

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PROFESSIONAL ELECTIVES COURSES (PEC)

SI.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C
1	P26VLP01	CAD for VLSI Circuits	PEC	3	0	0	3

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SEMESTER I

		Category: FC				
P26MA103	Graph Theory and Optimization Techniques	L	T	P	J	C
		2	0	2	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To introduce graph theory for modeling connectivity problems
- To enable linear programming and provide knowledge of nonlinear programming with KKT conditions
- To develop Monte Carlo simulation methods for stochastic modeling

COURSE OUTCOMES:

CO 1:	Model real-world systems using graph concepts (connectivity, paths, matrices) using Adjacency and incidence matrices without connectivity errors	**Apply**
CO 2:	Apply shortest path and MST algorithms for network optimization with correct path selection	**Apply**
CO 3:	Formulate linear programming models for resource allocation problems with optimal solution	**Apply**
CO 4:	Apply KKT conditions for constrained optimization problems under given constraints	**Apply**
CO 5:	Perform Monte Carlo simulation using MATLAB to estimate system parameters with 95% confidence	**Apply**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	3	2	1	-	-	-
CO 2	3	2	1	-	-	-
CO 3	3	2	1	-	-	-
CO 4	3	2	2	-	-	-
CO 5	2	2	2	-	-	-

SYLLABUS:

UNIT I: GRAPH BASICS **6 + 6**

Graphs – vertices, edges – Directed vs undirected – Bipartite, planar, complete graphs – Adjacency & incidence matrices – Graph isomorphism – Connectivity – Euler & Hamilton paths – Trees and spanning trees

UNIT II: GRAPH ALGORITHMS **6 + 6**

Directed graphs – Topological sorting – Shortest path algorithms (Dijkstra, Bellman-Ford) – DFS and BFS – Minimum spanning tree (Prim's, Kruskal) – Algorithm complexity basics

UNIT III: LINEAR PROGRAMMING **6 + 6**

Formulation of LP problems – Graphical solution – Simplex method – Transportation problem – Assignment problem – Duality concepts

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UNIT IV: NON-LINEAR PROGRAMMING **6 + 6**

T Constrained optimization – Equality and Inequality constraints – Karush-Kuhn-Tucker (KKT) conditions – Convex optimization basics

UNIT V: SIMULATION MODELLING **6 + 6**

Monte Carlo simulation – Static, Dynamic, Discrete, Continuous simulations – Random number generation – Random variate generation

LIST OF EXPERIMENTS

1. Graph Representation and Connectivity: VLSI Application: Modeling netlists and power grids • Create adjacency and incidence matrices • Plot graphs and find connected components
2. Shortest Path and Minimum Spanning Tree Algorithms: VLSI Application: Maze routing and clock distribution network • Implement Dijkstra's algorithm for shortest path • Implement Prim's algorithm for MST, compare both algorithms on the same graph
3. Linear Programming for Assignment: VLSI Application: Cell placement and pin assignment • Solve assignment problem using linprog and intlinprog • Solve transportation problem
4. Non-Linear Programming for Optimization: VLSI Application: Power minimization under delay constraints • Use fmincon for constrained optimization • Verify KKT conditions numerically
5. Monte Carlo Simulation: VLSI Application: SRAM cell stability analysis • Generate random numbers using rand() and randn() • Estimate parametric yield under process variations

CONTACT PERIODS:

Lecture: 30 Periods **Tutorial:** - Periods **Practical:** 30 Periods **Project:** - Periods **Total:** 60 Periods

TEXTBOOKS:

1. Douglas B. West, Introduction to Graph Theory, 2nd Edition, Pearson Education, 2015
2. Hamdy A. Taha, Operations Research: An Introduction, 10th Edition, Pearson, 2017
3. 3. P.K. Gupta and D.S. Hira, Operations Research, S. Chand and Company Ltd., 2022
4. MATLAB Documentation: Optimization Toolbox, Graph and Network Algorithms, The MathWorks, R2025b
5. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic Publishers, 2013

REFERENCES:

1. J.K. Sharma, Operations Research: Theory and Applications, 6th Edition, Macmillan Publishers, 2017
2. Richard Bronson, Schaum's Outline of Matrix Operations, 2nd Edition, McGraw-Hill, 2011
3. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer Berlin, 2011
4. Ahrens, M., Henke, D., Rabenstein, S. et al. Faster goal-oriented shortest path search for bulk and incremental detailed routing. Math. Program. 206, 3–32 (2024) https://doi.org/10.1007/s10107-023-01962-4
5. R. A. Solovyev et al., "PAGR: Accelerating Global Routing for VLSI Design Flow," in IEEE Access, vol. 13, pp. 6440-6450, 2025 DOI: 10.1109/ACCESS.2025.3526722

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SEMESTER I

		Category: PCC				
P26VL101	System Verilog Techniques	L	T	P	J	C
		3	0	0	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To learn System Verilog concepts to build and connect test benches
- To understand randomization concepts in System Verilog for effective test bench development
- To gain the knowledge in inter-process communication and functional coverage concepts in System Verilog

COURSE OUTCOMES:

CO 1:	IImplement SystemVerilog verification and data types for test bench development	**Apply**
CO 2:	Develop test benches using routines, interfaces, and assertions	**Apply**
CO 3:	Construct reusable verification environments using OOP and randomization	**Apply**
CO 4:	Analyze UVM environments and randomization strategies for design verification	**Analyze**
CO 5:	Examine communication mechanisms and coverage results for verification completeness	**Analyze**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2	1	3	2	2	1
CO 2	2	2	3	3	2	1
CO 3	3	2	3	3	3	2
CO 4	3	2	3	3	3	2
CO 5	3	2	3	3	3	3

SYLLABUS:

UNIT I: VERIFICATION GUIDELINES AND DATA TYPES 9

Verification Process – Basic Test Bench Functionality – Directed Testing – Methodology Basics – Constrained-Random Stimulus – Functional Coverage – Test Bench Components – Layered Test Bench – Building Layered Test Bench – Simulation Environment Phases – Maximum Code Reuse – Test Bench Performance –Data Types– Built-in Data Types – Fixed-Size Arrays – Dynamic Arrays – Queues – Associative Arrays – Linked Lists – Array Methods – Choosing a Storage Type – Creating New Types with `typedef` – Creating User-Defined Structures – Type Conversion – Enumerated Types – Constants – Strings – Expression Width

UNIT II: ROUTINES AND CONNECTING THE TEST BENCH & DESIGN 9

Procedural Statements – Tasks – Functions and Void Functions – Routine Arguments – Returning from Routine – Local Data Storage – Time Values– Connecting the Test Bench and Design–Separating the Test Bench and Design – Interface Constructs – Stimulus Timing – Interface Driving and Sampling – Connecting It All Together – Top-Level Scope – Program–Module Interactions – SystemVerilog Assertions

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UNIT III: BASIC OOP 9

Introduction – First Class – Defining a Class – OOP Terminology – Creating New Objects – Object De-allocation – Using Objects – Static Variables vs. Global Variables – Class Methods – Defining Methods Outside the Class – Scoping Rules – Using One Class Inside Another – Dynamic Objects – Copying Objects – Public vs. Private – Straying Off Course – Building a Test Bench

UNIT IV: RANDOMIZATION AND UVM 9

Introduction – Randomization – Randomization in SystemVerilog – Constraint Details – Solution Probabilities – Controlling Multiple Constraint Blocks – Valid Constraints – In-Line Constraints – `pre_randomize` and `post_randomize` Functions – Constraint Tips and Techniques – Common Randomization Problems –**UVM:** Specification – Feature Extraction – Stimulus Generation Plan – Coverage Plan – Verification Environment – Scoreboard

UNIT V: INTERPROCESS COMMUNICATION AND FUNCTIONAL COVERAGE 9

Interprocess Communication – Events – Semaphores – Mailboxes –Functional Coverage –Coverage Types – Functional Coverage Strategies – Simple Functional Coverage Example – Anatomy of a Cover Group – Triggering a Cover Group – Data Sampling – Cross Coverage – Generic Cover Groups – Coverage Options – Analyzing Coverage Data – Measuring Coverage Statistics During Simulation

CONTACT PERIODS:

Lecture: 45 Periods **Tutorial:** - Periods **Practical:** - Periods **Project:** - Periods **Total:** 45 Periods

TEXTBOOKS:

1. Chris Spears, System Verilog for Verification , 2nd Edition, Springer, 2008
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006

REFERENCES:

1. Vijayaraghavan, Srikanth, and Meyyappan Ramanathan. A practical guide for SystemVerilog assertions , Springer Science & Business Media, 2006
2. Bergeron, Janick. Writing testbenches using SystemVerilog , 1st Edition,Springer Science & Business Media, 2007
3. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010

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SEMESTER I

		Category: PCC				
P26VL102	Semiconductor Device Modeling	L	T	P	J	C
		3	0	0	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To understand MOSFET device physics and characteristics
- To study MOSFET modeling, scaling, and key parameters
- To learn about CMOS performance and device effects

COURSE OUTCOMES:

CO 1:	Demonstrate MOSFET device characteristics under capacitance, charge, breakdown, and high-field conditions	**Apply**
CO 2:	Implement MOSFET models and numerical methods for device and circuit analysis	**Apply**
CO 3:	Utilize MOSFET scaling principles to assess threshold voltage and channel characteristics	**Apply**
CO 4:	Analyze MOSFET parameters and parasitic elements influencing device performance	**Analyze**
CO 5:	Assess CMOS performance variations due to device, parasitic, transport, and temperature effects	**Analyze**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2	1	3	2	2	1
CO 2	3	2	3	3	2	2
CO 3	2	1	3	3	3	2
CO 4	3	2	3	3	3	2
CO 5	3	2	3	3	3	3

SYLLABUS:

UNIT I: MOSFET DEVICE PHYSICS 9

Capacitances in MOS structure – Polysilicon gate work function and depletion effects – Charge in silicon dioxide – Effect of interface traps and oxide charge on device characteristics – Current-voltage characteristics of a Schottky barrier diode – Impact ionization and avalanche Breakdown – Band-to-band tunneling in MOSFET – Injection of hot carriers from silicon into silicon dioxide – High-field effects in gated diode

UNIT II: MOSFET MODELING 9

Long channel MOSFETs – Sub-threshold characteristics – Short channel MOSFETs – Velocity saturation and high-field transport channel length modulation – MOSFET degradation and breakdown at high fields – Device simulations in VLSI – Nodal, mesh, modified nodal and hybrid analysis equations – Solution of nonlinear networks through Newton-Raphson technique – Convergence and stability

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UNIT III: SCALING EFFECTS 9

MOSFET Scaling – Constant-field scaling – Generalized scaling – Non-scaling effects – Threshold voltage requirement – Channel profile design – Non-uniform doping – Quantum effect on threshold voltage – Discrete dopant effects on threshold voltage

UNIT IV: MOSFET KEY PARAMETERS 9

MOSFET channel length – Extraction of effective channel length by C-V measurements – Transconductance of MOSFET – CMOS parasitic elements – Source-drain resistance – Parasitic capacitances – Gate resistance – Interconnect R and C

UNIT V: CMOS PERFORMANCE METRICS 9

Sensitivity of CMOS delay to device parameters – Delay sensitivity to channel width, length, and gate oxide thickness, supply voltage and threshold voltage – Sensitivity of delay to parasitic resistance and capacitance – Performance factors of advanced CMOS devices – Effect of Transport Parameters on CMOS Performance – Low-Temperature CMOS

CONTACT PERIODS:

Lecture: 45 Periods **Tutorial:** - Periods **Practical:** - Periods **Project:** - Periods **Total:** 45 Periods

TEXTBOOKS:

1. Yuan Taur, TakH Ning, "Fundamentals of Modern VLSI Devices", 2nd edition, Cambridge University Press, 2013
2. B.G Streetman and S.K Banerjee, "Solid State Electronic Devices", 7th edition, Prentice Hall India, 2015

REFERENCES:

1. J P Collinge, C A Collinge, "Physics of Semiconductor Devices", 2nd edition, Springer, 2006
2. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", 1st edition, John Wiley & Sons Ltd., 2003
3. S.M. Sze Kwok K. Ng, "Physics of Semiconductor Devices", 2nd edition, John Wiley & Sons, 2007
4. Arora, Narain D. "Fundamentals of Microelectronics", 2nd edition, Wiley Student Edition, 2013

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SEMESTER I

		Category: PCC				
P26VL103	Digital System Design with AI for VLSI	L	T	P	J	C
		3	0	0	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To understand algorithm-to-architecture mapping and digital design techniques
- To study logic, sequential, datapath, and memory architectures
- To explore AI-assisted optimization and reconfigurable computing

COURSE OUTCOMES:

CO 1:	Apply algorithm-to-architecture mapping techniques for digital system design	**Apply**
CO 2:	Develop combinational circuits using logic minimization and power-delay reduction techniques	**Apply**
CO 3:	Implement sequential and datapath architectures using AI-assisted design techniques	**Apply**
CO 4:	Analyze power, performance, area, timing, and reliability trade-offs in VLSI systems	**Analyze**
CO 5:	Examine reconfigurable architectures and FPGA-based AI acceleration techniques	**Analyze**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2	1	3	3	2	1
CO 2	1	1	3	3	2	1
CO 3	2	1	3	3	3	2
CO 4	3	1	3	3	2	2
CO 5	2	1	3	3	3	3

SYLLABUS:

UNIT I: ALGORITHM TO ARCHITECTURE MAPPING 9

Mapping algorithms into digital architectures – Datapath synthesis and control structures – Critical path and timing analysis – Finite State Machines (FSM) – Hazards and reliability in digital circuits

UNIT II: COMBINATIONAL LOGIC DESIGN & OPTIMIZATION 9

Combinational circuit delay modeling – Power and energy optimization techniques – Logic minimization and technology mapping – Clocking methodologies and performance metrics – Static and dynamic optimization strategies

UNIT III: SEQUENTIAL DESIGN AND AI-ASSISTED OPTIMIZATION 9

Design of latches and flip-flops – Sequential circuit timing and synchronization – Sequential design methodologies – Introduction to Machine Learning for VLSI– AI-based timing prediction and delay estimation –AI-assisted fault detection in sequential circuits

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UNIT IV: AI-ENABLED DATAPATH AND MEMORY SYSTEMS **9**

Datapath design – Arithmetic units: Addition, subtraction – Comparators, coding –Multiplication architectures – AI-based power, area, and delay estimation, Memory systems: SRAM, DRAM, ROM – AI-based fault detection in memory systems

UNIT V: RECONFIGURABLE COMPUTING AND AI APPLICATIONS **9**

Fine-grain and coarse-grain architectures – Configuration architectures – Single-context and multi-context systems – Partially reconfigurable systems – Parallel processing concepts – AI acceleration using FPGA

CONTACT PERIODS:

Lecture: 45 Periods **Tutorial:** - Periods **Practical:** - Periods **Project:** - Periods **Total:** 45 Periods

TEXTBOOKS:

1. Harris, D., & Weste, N, CMOS VLSI Design, 4th edition, Pearson Education, 2010
2. Wolf W, FPGA-Based System Design, 1st edition, Pearson Education, 2004

REFERENCES:

1. C. Roth, Fundamentals of Digital Logic Design, 6th edition Jaico, 2009
2. C. Bobda, Introduction to Reconfigurable Computing, 1st edition,Springer, 2007
3. 4. Elfadel, I. A. M., Boning, D. S., & Li, X.. Machine learning in VLSI computer-aided design. 1st edition,Springer, 2019

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SEMESTER I

		Category: RMC				
P26RMC01	Research Methodology and IPR (Common to CAD, DS, ES, PCS, PHDCE, PHDIC, PHDME, PHDSH, SE, VL)	L	T	P	J	C
		3	0	0	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To impart knowledge in problem formulation, analysis and solutions
- To impart skills required for technical paper writing / presentation without violating professional ethics
- To familiarize knowledge on patent drafting and filing patents

COURSE OUTCOMES:

CO 1:	Apply the principles of research problem formulation to identify, define, and investigate engineering research problems using appropriate data collection and analysis techniques	**Apply**
CO 2:	Analyze research literature, data collection methods, research ethics, and plagiarism issues to identify research gaps and select suitable methodologies	**Analyze**
CO 3:	Evaluate the quality of technical reports, research papers, and research proposals by applying standard scientific writing and presentation practice	**Evaluate**
CO 4:	Apply the principles and procedures of Intellectual Property Rights (IPR), including patents, patent filing, and international patenting systems, to protect technological innovation	**Apply**
CO 5:	Evaluate patent rights, technology transfer mechanisms, patent databases, geographical indications, and emerging developments in Intellectual Property Rights for engineering and research applications	**Evaluate**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	3	-	-	-	-	-
CO 2	3	-	-	-	-	-
CO 3	3	3	-	-	-	-
CO 4	-	3	-	-	-	2
CO 5	-	3	-	-	-	2

SYLLABUS:

UNIT I: RESEARCH PROBLEM FORMULATION 9

Meaning of research problem – Sources of research problem – Criteria characteristics of a good research problem – Errors in selecting a research problem – Scope and objectives of research problem. Approaches of investigation of solutions for research problem – Data collection – Analysis – Interpretation – Necessary instrumentations

UNIT II: LITERATURE REVIEW AND DATA COLLECTION 9

Effective literature studies approaches – Analysis – Plagiarism and research ethics. Method of data collection – Types of data – Primary Data – Scales of measurement – Source and collection of data observation method – Secondary data

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UNIT III: TECHNICAL WRITING / PRESENTATION 9

Effective technical writing: How to write report – Paper – Developing a research proposal – Format of research proposal – Presentation and assessment by a review committee

UNIT IV: INTRODUCTION TO INTELLECTUALPROPERTY RIGHTS 9

Nature of Intellectual Property: Patents – Designs – Trade and Copyright. Process of Patenting and Development – technological research – Innovation – Patenting – Development – International Scenario – International cooperation on Intellectual Property – Procedure for grants of patents – Patenting under PCT

UNIT V: INTELLECTUAL PROPERTYRIGHTS 9

Patent Rights: Scope of Patent Rights – Licensing and transfer of technology – Patent information and databases – Geographical Indications – New Developments in IPR – Administration of Patent System – IPR of Biological Systems – Computer Software etc.

CONTACT PERIODS:

Lecture: 45 Periods **Tutorial:** - Periods **Practical:** - Periods **Project:** - Periods **Total:** 45 Periods

REFERENCES:

1. Cooper, DR and Schindler, P S., "Business Research Methods", 9th edition, Tata McGraw Hill, 2014
2. Robert P.Merges, Peter S, Menell, Mark A.Lemley, "Intellectual Property in New Technological age", Volume I, Clause 8 Publishing,2022
3. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", 3rd edition, Sage Publications,2010

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SEMESTER I

		Category: PCC				
P26VL104	HDL Programming Laboratory	L	T	P	J	C
		0	0	4	0	2

QP PATTERN: B

COURSE OBJECTIVES:

- To learn Verilog and System Verilog concepts to design and implement digital modules and test benches.
- To verify hardware designs using randomization, assertions, and functional coverage techniques
- To develop structured and UVM-based verification environments for complex digital systems

COURSE OUTCOMES:

CO 1:	Implement digital designs and testbenches using SystemVerilog constructs	**Apply**
CO 2:	Apply constrained randomization, functional coverage, and verification techniques to validate designs	**Apply**
CO 3:	Analyze design functionality using sequences and UVM-based verification environments	**Analyze**
CO 4:	Demonstrate individual competency or effective teamwork in designing and implementing the experimental results	**Apply**
CO 5:	Apply ethical standards and present experimental results effectively	**Apply**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	2	1	3	2	2	1
CO 2	2	2	3	3	2	1
CO 3	3	2	3	3	3	2
CO 4	3	2	3	3	3	2
CO 5	3	2	3	3	3	3

SYLLABUS:

LIST OF EXPERIMENTS

1. Develop 8X1 mux using verilog code in design.sv and develop Test bench for 8X1 mux in testbench.sv with different inputs at various times.
2. Write a program to demonstrate two-state and four-state data types
3. Write a program to demonstrate push_front, pop_front, push_back and pop_back with respect to Queues
4. Design a full adder using the interface construct to model inter-module communication
5. Create a program to highlight the difference between rand and randc constructs in constrained randomization
6. Build a 8-bit adder and verify its functionality using a structured verification environment
7. Design a UART module using SystemVerilog
8. Design, simulate, and analyze functional coverage to ensure thorough verification of a given design
9. Design and simulate a verification test that exercises multiple sequences
10. Create and simulate a configurable Universal Verification Methodology (UVM) test environment

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CONTACT PERIODS:

Lecture: - Periods	**Tutorial:** - Periods	**Practical:** 30 Periods	**Project:** - Periods	**Total:** 30 Periods

REFERENCES:

1. nil

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Learn Beyond

PROFESSIONAL ELECTIVE COURSES

		Category: PEC				
P26VLP01	CAD for VLSI Circuits	L	T	P	J	C
		3	0	0	0	3

QP PATTERN: B

COURSE OBJECTIVES:

- To understand the basic concepts of physical design and algorithms techniques
- To learn floor planning and routing
- To study simulation and high-level synthesis

COURSE OUTCOMES:

CO 1:	Apply graph algorithms to represent and solve VLSI design problems	**Apply**
CO 2:	Choose appropriate algorithm for partitioning and placement	**Apply**
CO 3:	Develop floor planning and routing solutions using suitable algorithms	**Apply**
CO 4:	Examine the optimized gate level representation of combinational circuits	**Analyze**
CO 5:	Analyze high-level synthesis techniques involving scheduling, allocation, and assignment	**Analyze**

CO - PO MAPPING:

Particular	PO1	PO2	PO3	PO4	PO5	PO6
CO 1	3	1	2	3	2	1
CO 2	2	1	3	3	3	2
CO 3	2	1	3	3	3	2
CO 4	3	1	3	3	2	1
CO 5	2	1	3	3	3	2

SYLLABUS:

UNIT I: DESIGN METHODOLOGIES AND GRAPH THEORY ALGORITHMS 9

Introduction to VLSI design flow and design methodologies – Evolution of CAD tools – Classification of CAD tools –Data structures for representation of graph– Computational complexity – Examples of graph algorithm – Depth first search – Breadth first search – Dijkstra's shortest path algorithm

UNIT II: LAYOUT COMPACTION, PLACEMENT AND PARTITIONING 9

Design rules – Symbolic layout – Problem formulation – Algorithms for constraint graph compaction – The Liao-Wong algorithm –The Bellman-Ford algorithm – Circuit representation – Wire length estimation –Placement algorithms – Partitioning – The Karnighan-Lin partitioning algorithm

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UNIT III: FLOOR PLANNING AND ROUTING **9**

Floor planning concepts – Shape functions – Floor plan sizing – Classification of floor planning algorithms – Constraint based floor planning – Classification of global routing algorithms – Maze routing algorithms – Lee's algorithm – Line-probe algorithms – Shortest path based algorithms

UNIT IV: SIMULATION AND LOGIC SYNTHESIS **9**

Gate level modeling and simulation – Switch level modeling and simulation – Combinational logic synthesis – Binary decision diagram – ROBDD principles – Implementation and manipulation – Variable ordering – Applications to verification and combinational optimization

UNIT V: HIGH LEVEL SYNTHESIS **9**

Hardware models – Internal representation – Allocation – Assignment and scheduling – Simple scheduling algorithm – Assignment problem– High-level transformations

CONTACT PERIODS:

Lecture: 45 Periods **Tutorial:** - Periods **Practical:** - Periods **Project:** - Periods **Total:** 45 Periods

TEXTBOOKS:

1. Sabih H, Gerez.,"Algorithms for VLSI Design Automation" 3rd edition, John Wiley & Sons., 2008
2. Sherwani, N.A.,"Algorithms for VLSI Physical Design Automation", 3rd edition, Kluwer Academic Publishers, 2002

REFERENCES:

1. Charles J. Alpert , Dinesh P. Mehta, Sachin S. Sapatnekar,"Handbook of Algorithms for Physical Design Automation", 1st edition, CRC Press, 2009
2. Stephen Trimberger, "Introduction to CAD for VLSI", 2nd edition, Kluwer Academic Publisher, 2002
3. Sadiq M.Sait, Habib Youssef, VLSI Physical Design Automation: Theory and Practice", 2nd edition, World Scientific, 1999

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